

FIG.1

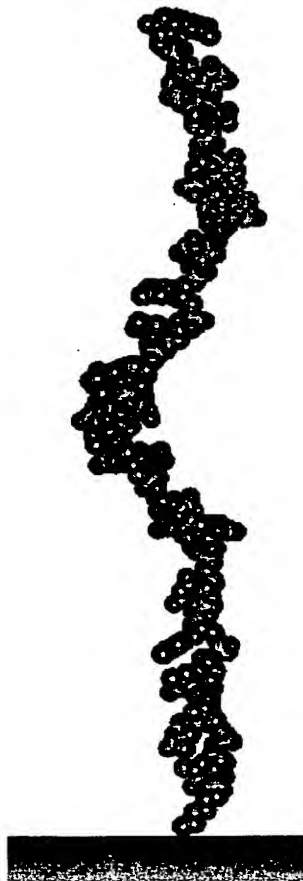
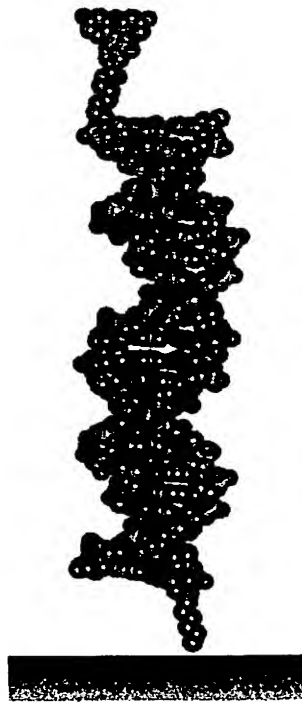


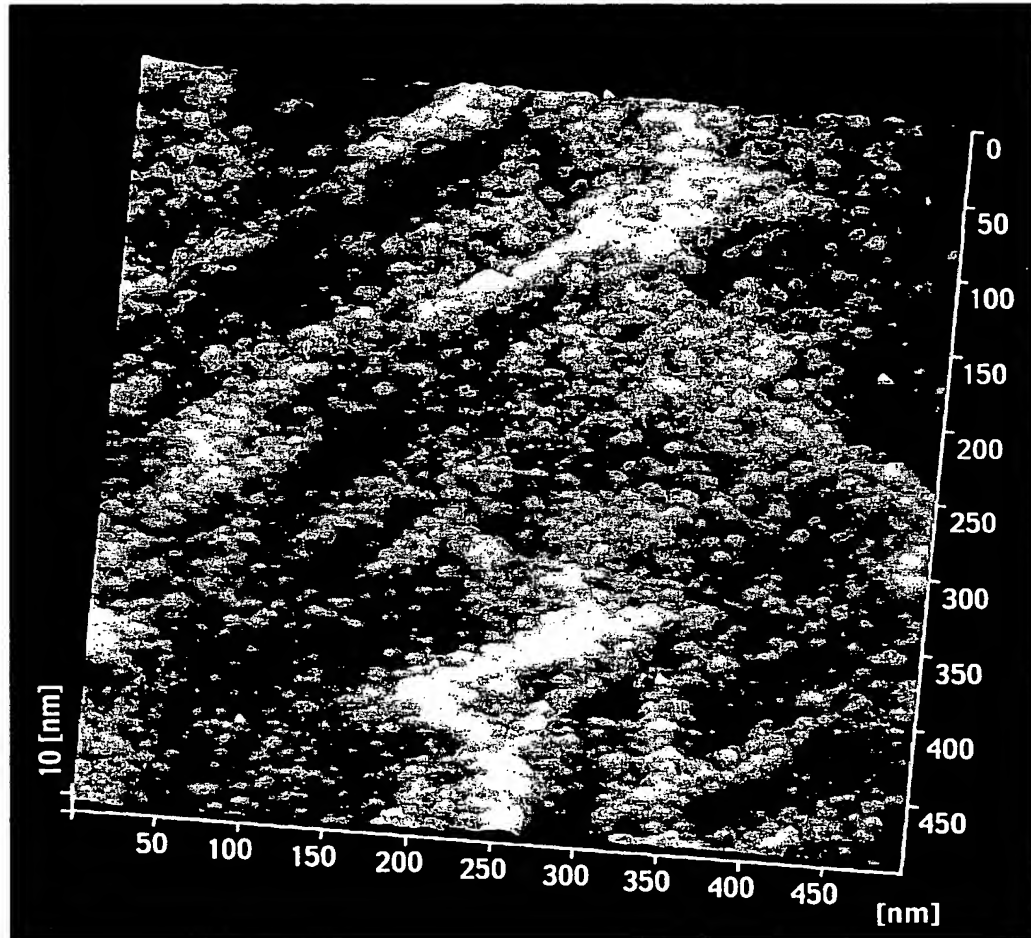
FIG.2



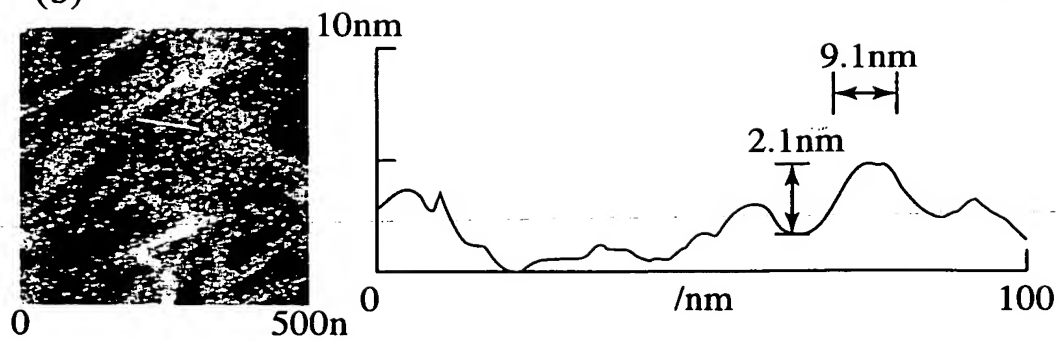
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FIG.3

(a)



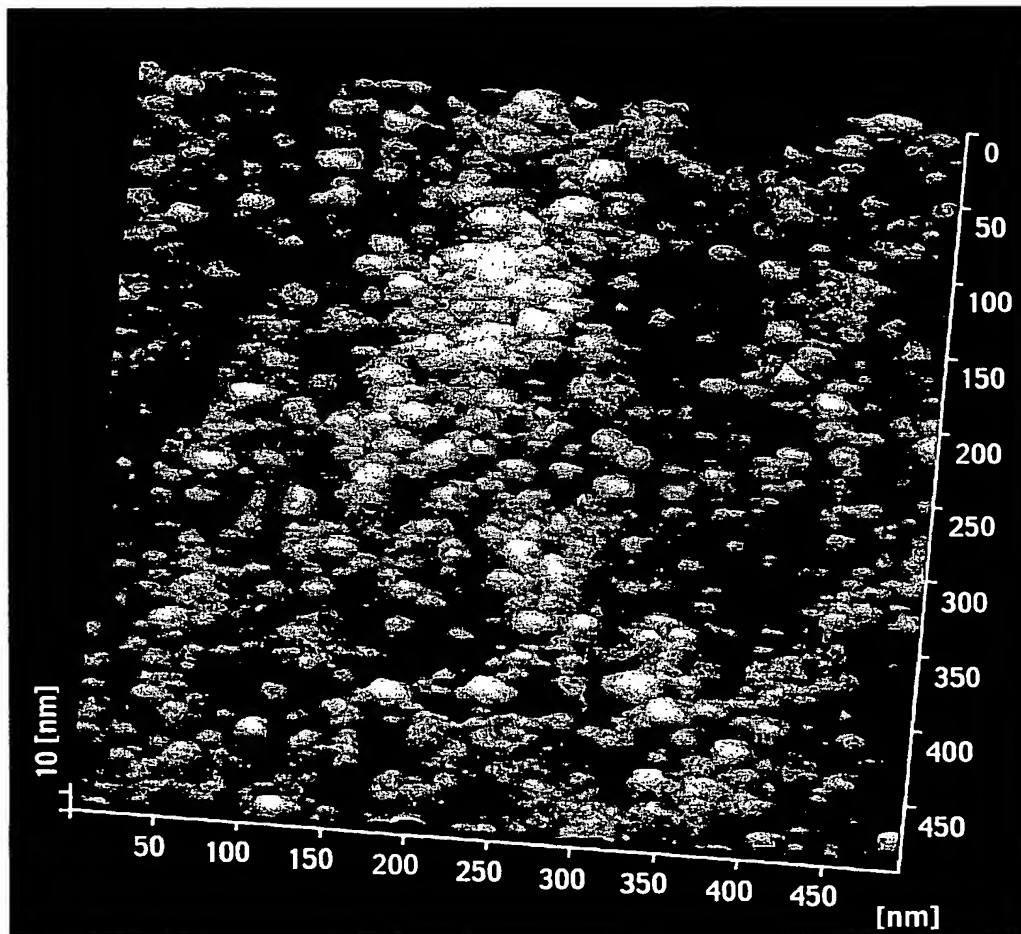
(b)



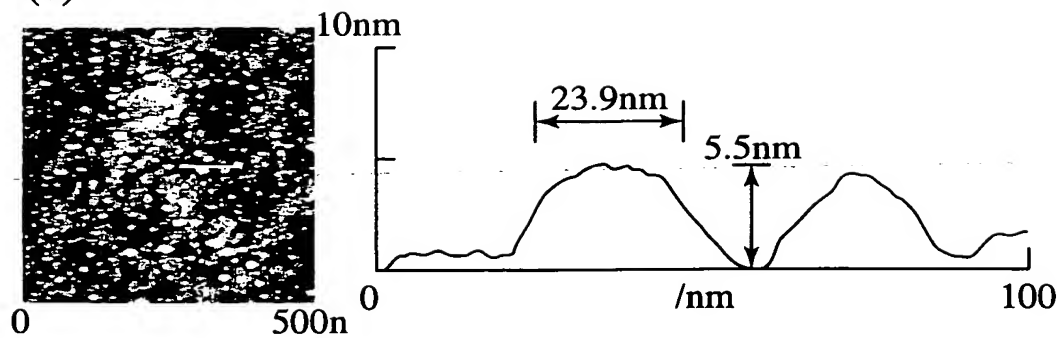
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FIG.4

(a)



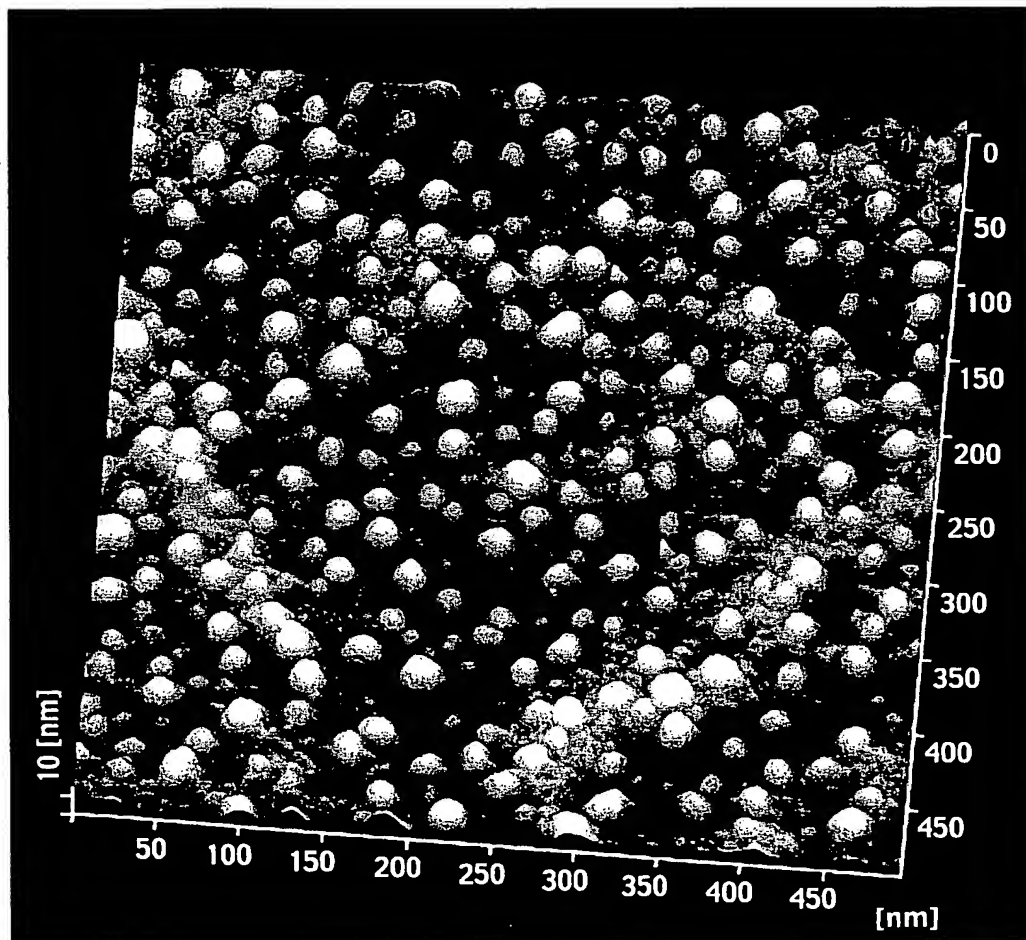
(b)



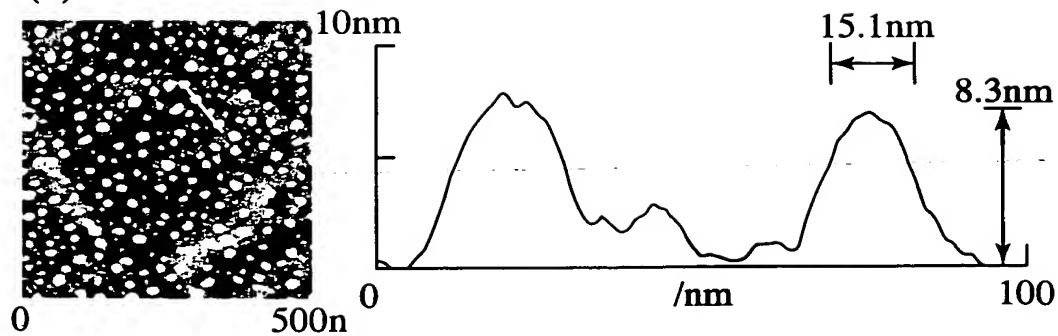
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FIG.5

(a)



(b)



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FIG. 6

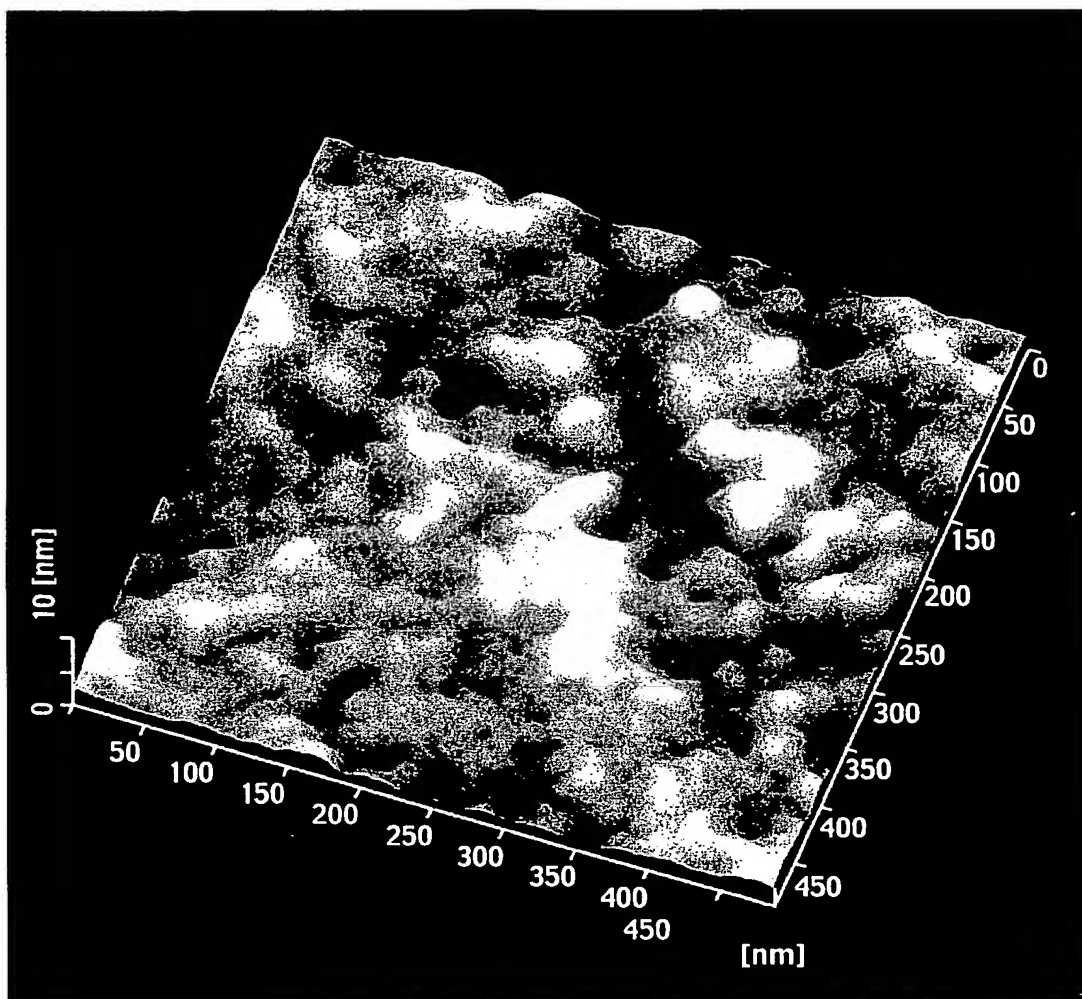
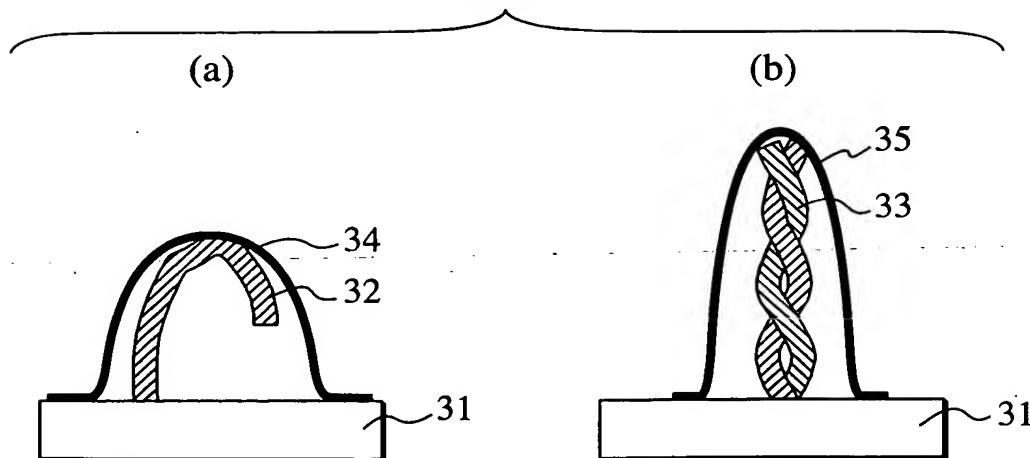


FIG. 7



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FIG.8

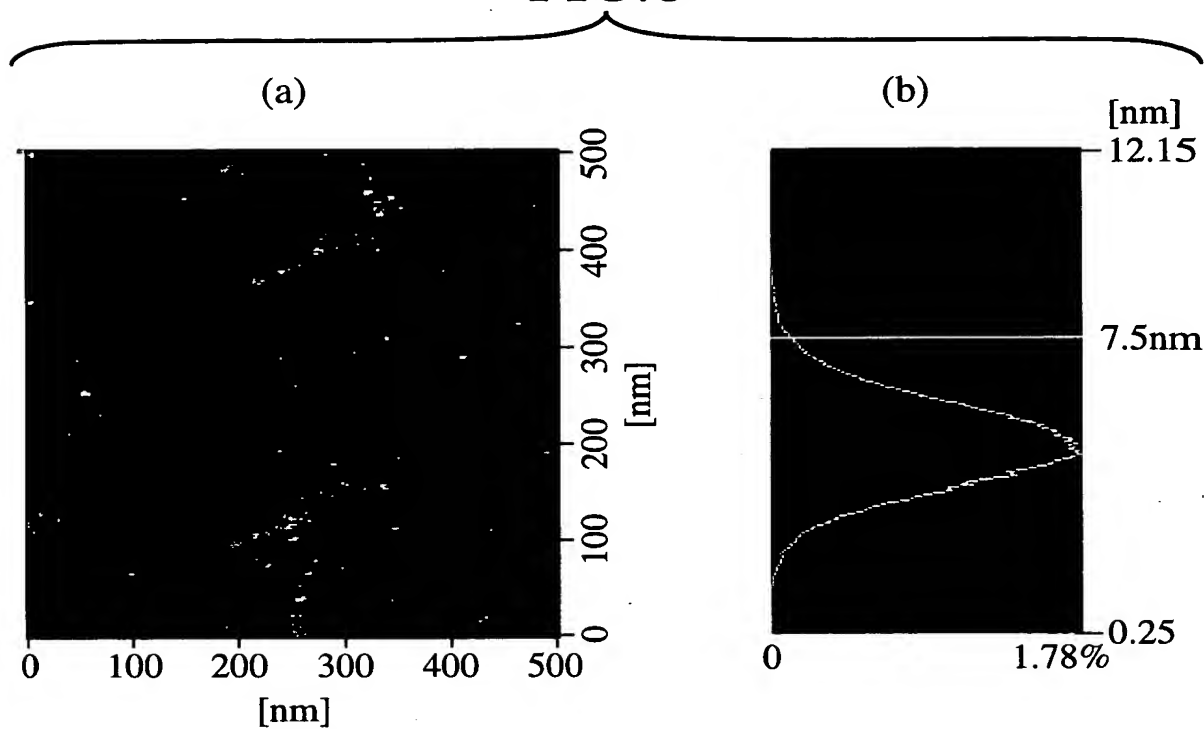
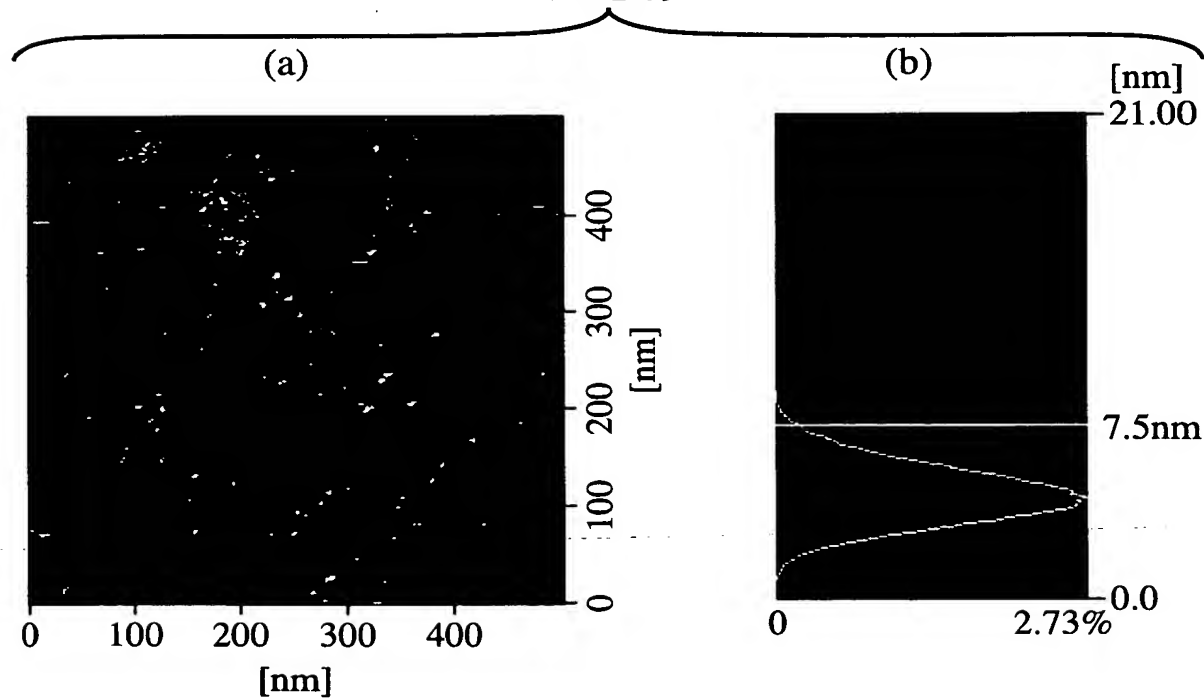


FIG.9



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FIG. 10

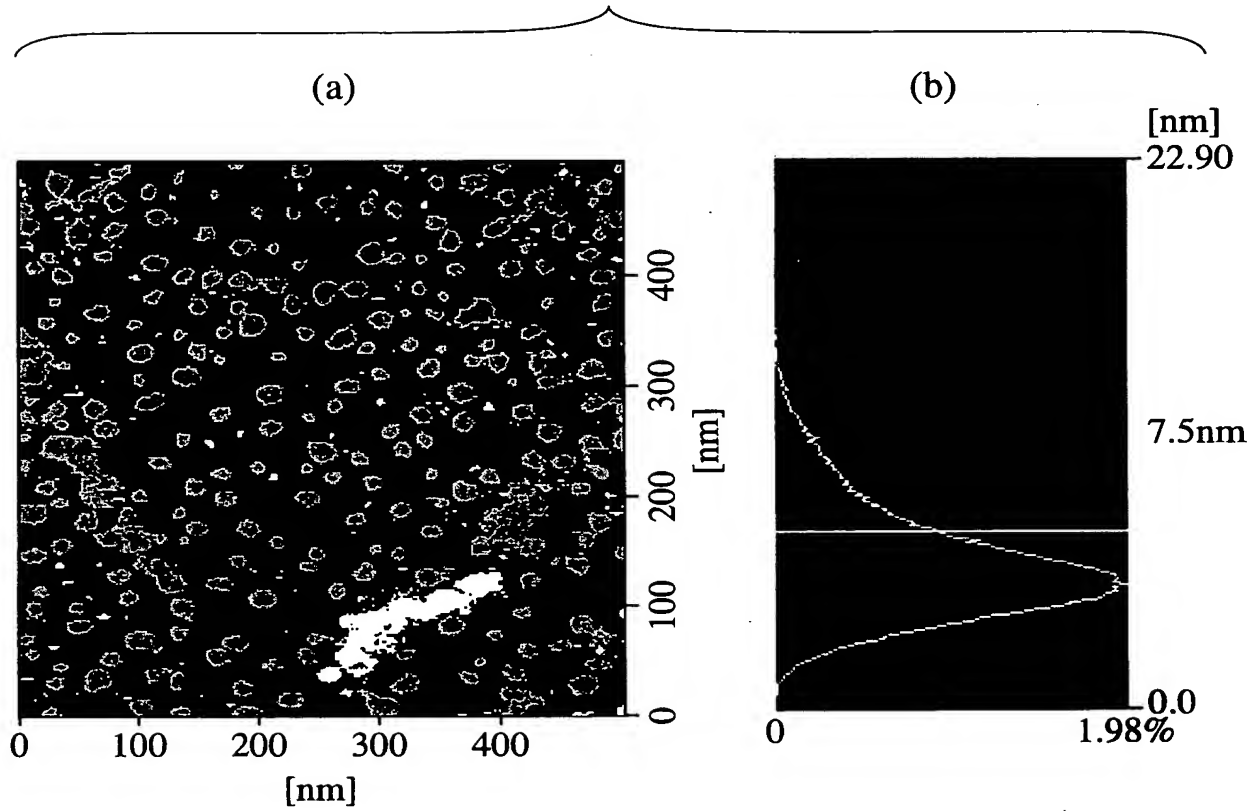


FIG. 11

13 ELECTRICAL SIGNAL AMPLIFIER

12 LASER LIGHT DETECTOR

8 LASER LIGHT SOURCE

10

9

11

2

4

1 SUBSTRATE

3

5 DRIVE MECHANISM

6 DRIVE MECHANISM

7 DRIVE CONTROL CIRCUIT

14 COMPUTER

15 DISPLAY

The block diagram illustrates the system architecture. A **DRIVE CONTROL CIRCUIT** (23) is connected to a **COMPUTER** (24). The **DRIVE CONTROL CIRCUIT** (23) is also connected to a **DRIVE MECHANISM** (20) and a **TUNNEL CURRENT DETECTOR** (22). The **COMPUTER** (24) is connected to a **DISPLAY** (25). The **DRIVE MECHANISM** (20) is connected to a **CONTAINER** (17), which contains a **SUBSTRATE** (16). The **CONTAINER** (17) is also connected to a **VOLTAGE GENERATOR** (21). The **TUNNEL CURRENT DETECTOR** (22) is connected to the **VOLTAGE GENERATOR** (21). The **VOLTAGE GENERATOR** (21) is connected to the **SUBSTRATE** (16).

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FIG. 13

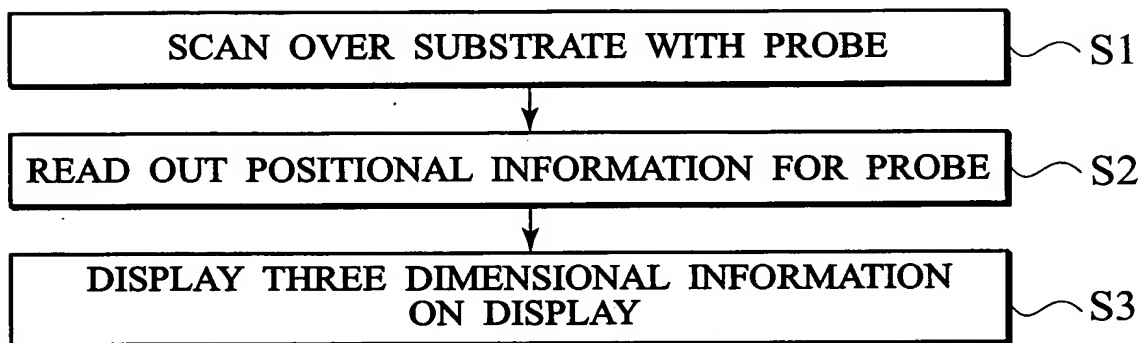
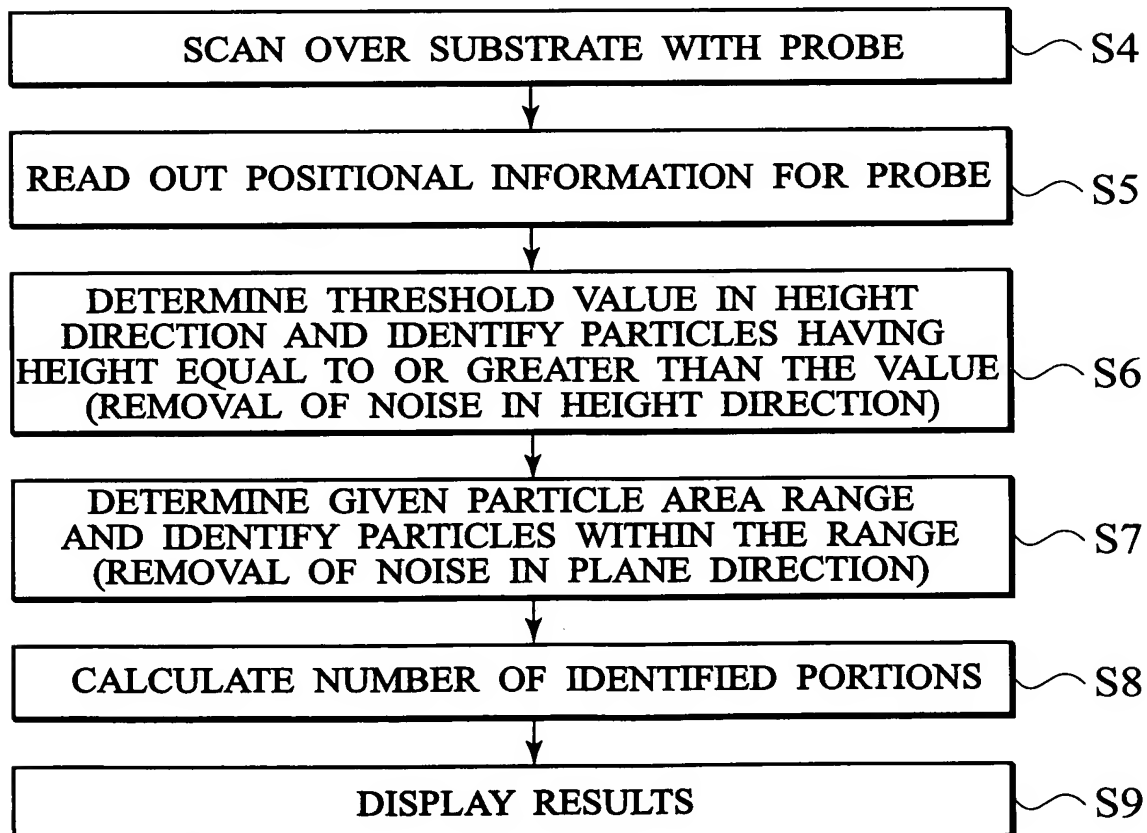
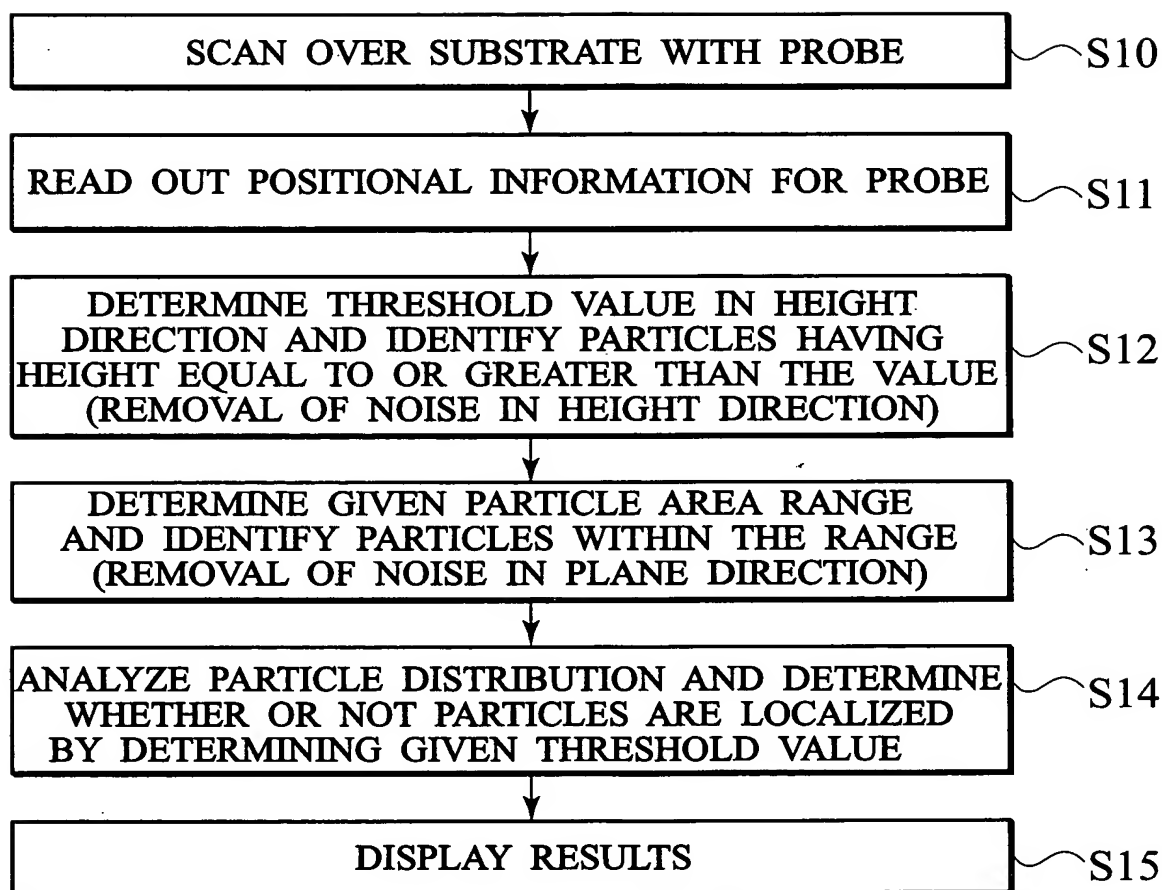


FIG. 14



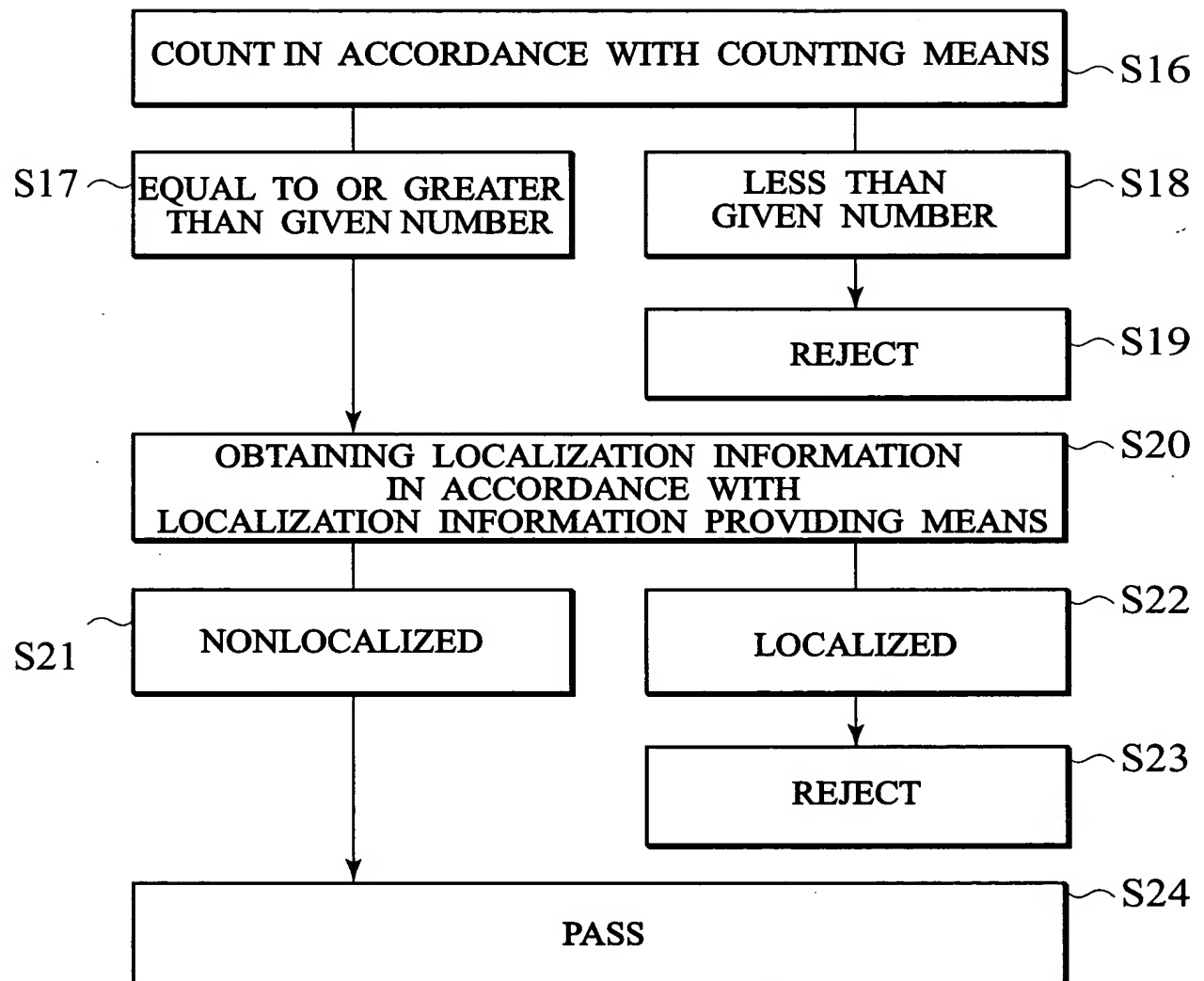
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FIG. 15



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FIG. 16



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FIG.17

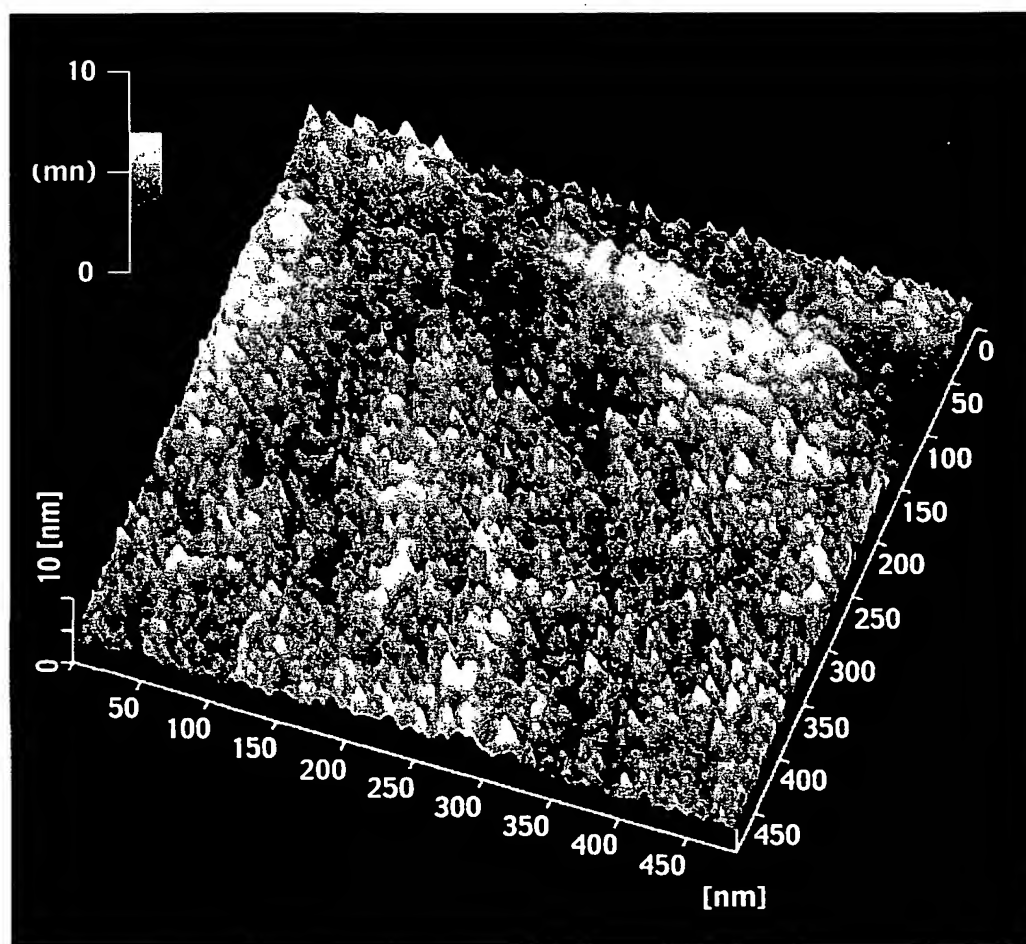


FIG.18

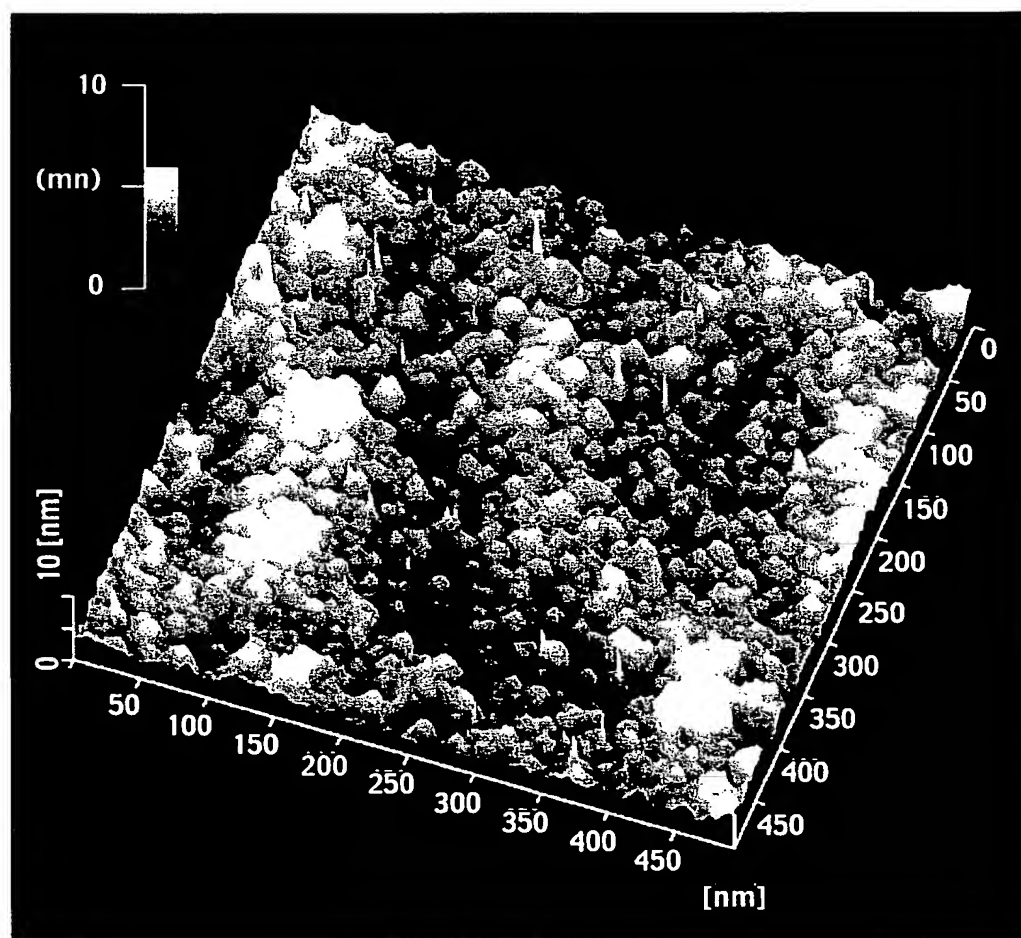
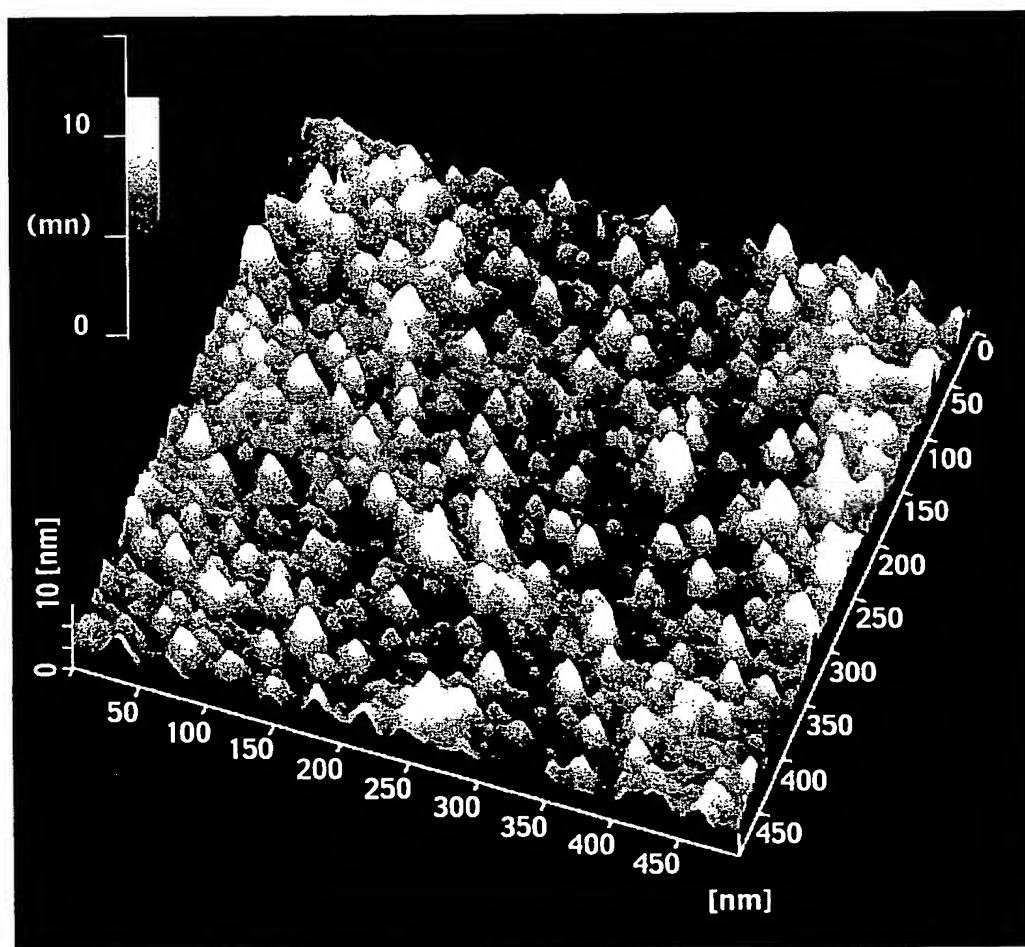


FIG.19



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FIG.20

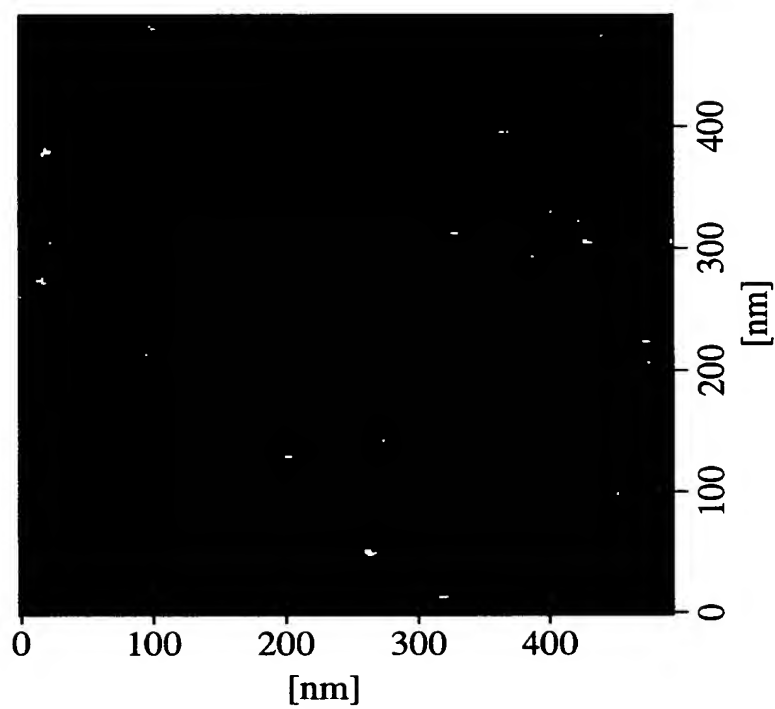
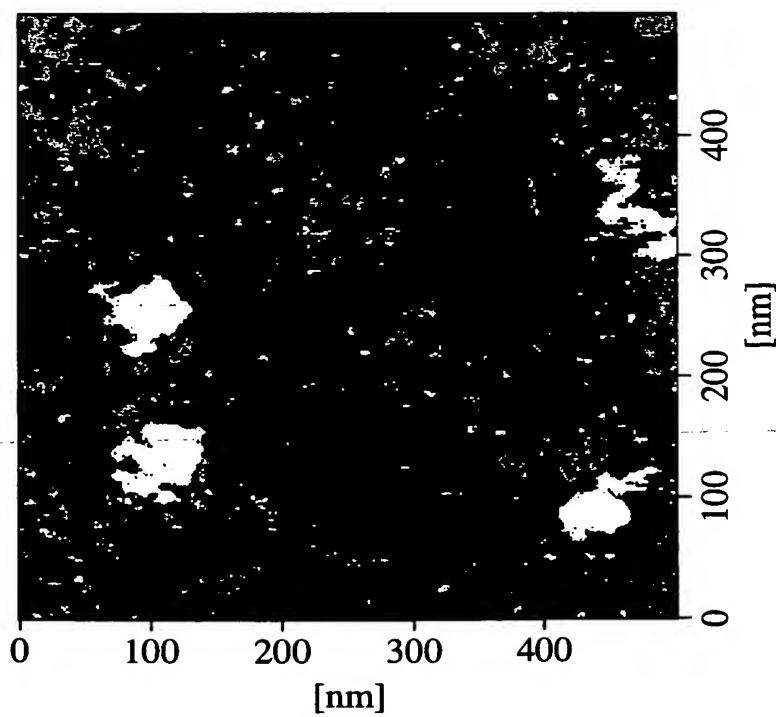


FIG.21



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FIG.22

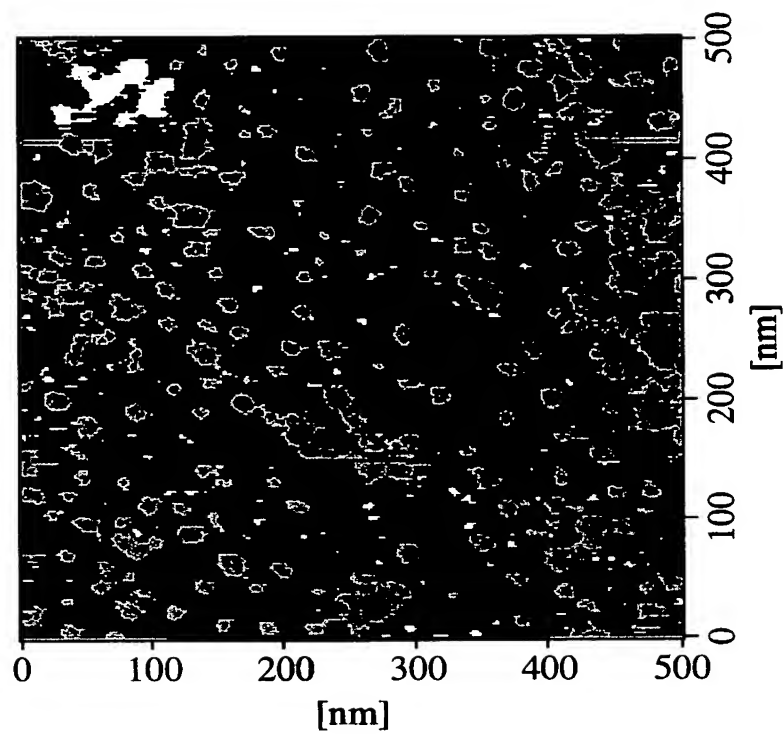
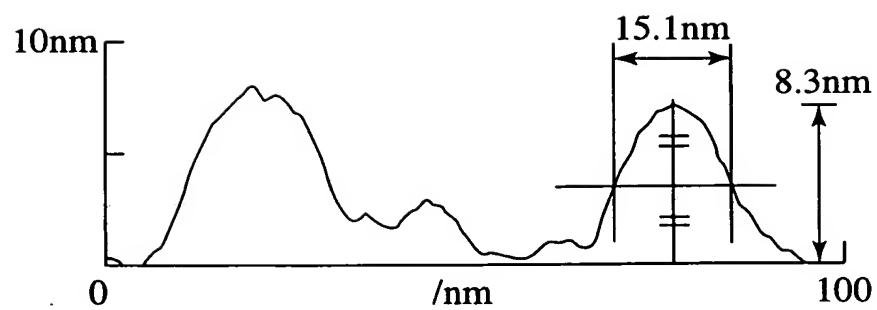


FIG.23



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FIG.24

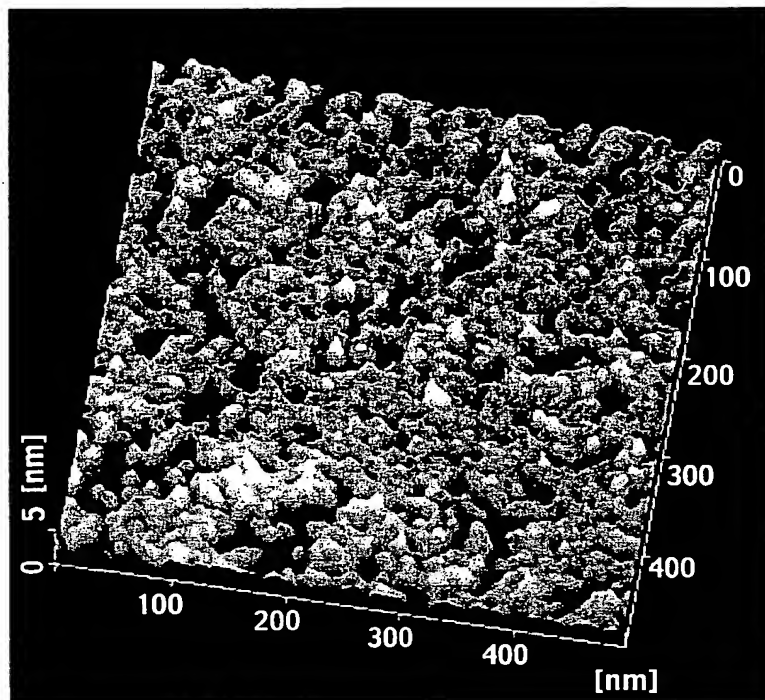


FIG.25

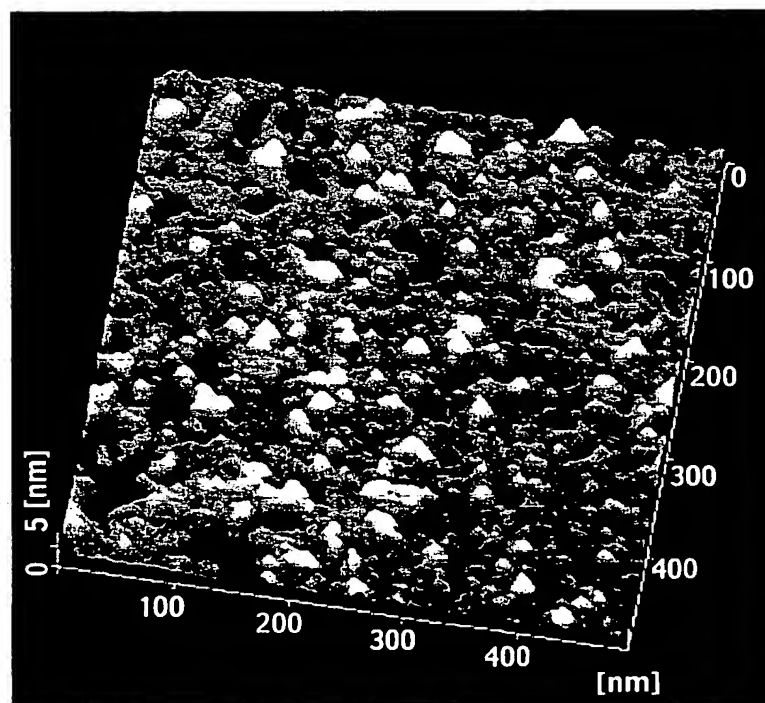


FIG.26

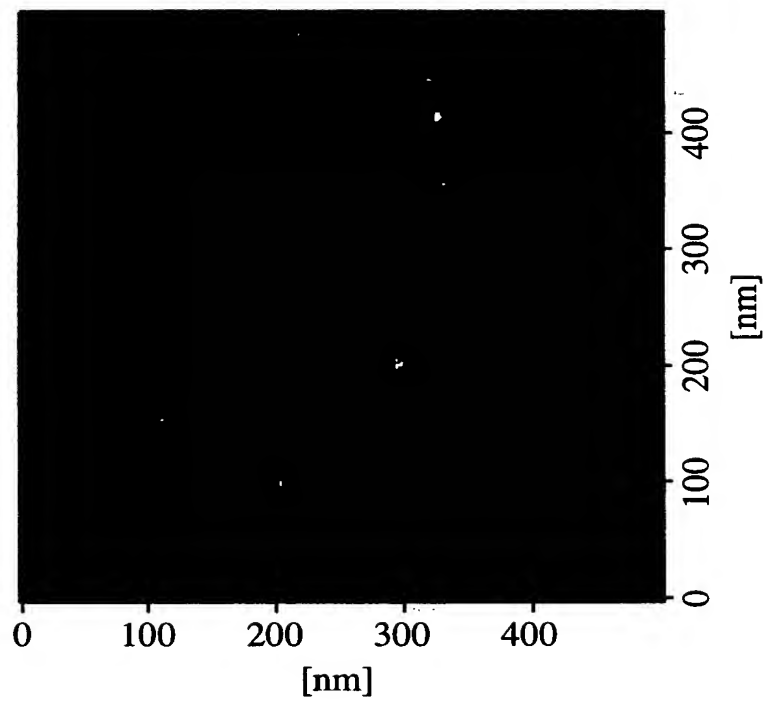


FIG.27

